N-Channel and P-Channel 12 V (D-S) MOSFET

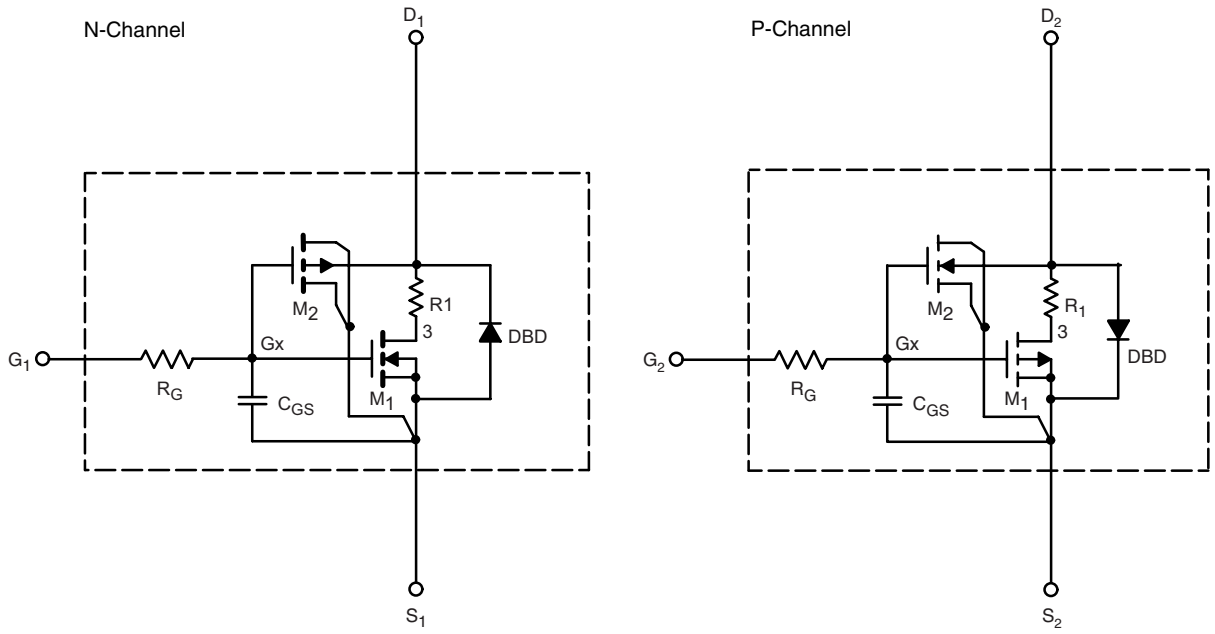
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

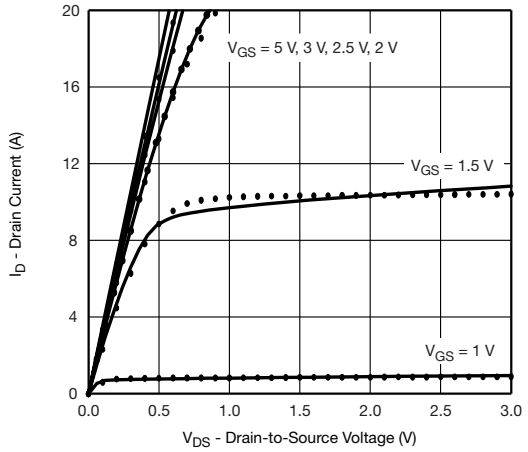
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.46	-	V
		V_{DS} = V_{GS}, I_D = - 250 µA	P-Ch	0.74	-	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.6 A	N-Ch	0.028	0.028	Ω
		V_{GS} = - 4.5 V, I_D = - 3.6 A	P-Ch	0.048	0.048	
		V_{GS} = 2.5 V, I_D = 4.2 A	N-Ch	0.032	0.032	
		V_{GS} = - 2.5 V, I_D = - 3.1 A	P-Ch	0.066	0.066	
Forward Transconductance[a]	g_{fs}	V_{DS} = 6 V, I_D = 4.6 A	N-Ch	20	21	S
		V_{DS} = - 6 V, I_D = - 3.6 A	P-Ch	10	11	
Diode Forward Voltage[a]	V_{SD}	I_S = 4.8 A,	N-Ch	0.88	0.85	V
		I_S = - 3.7	P-Ch	0.86	- 0.87	
Dynamic[b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 6 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 6 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	417	420	pF
			P-Ch	523	545	
Output Capacitance	C_{oss}		N-Ch	100	100	
			P-Ch	201	192	
Reverse Transfer Capacitance	C_{rss}		N-Ch	60	62	
			P-Ch	176	175	
Total Gate Charge	Q_g	V_{DS} = 6 V, V_{GS} = 10 V, I_D = 5.9 A	N-Ch	8.3	10	nC
		V_{DS} = - 6 V, V_{GS} = - 10 V, I_D = - 4.7 A	P-Ch	12	13	
		N-Channel V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 5.9 A P-Channel V_{DS} = - 6 V, V_{GS} = - 4.5 V, I_D = - 4.7 A	N-Ch	4	5.6	
			P-Ch	6	7.8	
Gate-Source Charge	Q_{gs}		N-Ch	0.70	0.70	
			P-Ch	1.3	1.3	
Gate-Drain Charge	Q_{gd}		N-Ch	0.85	0.85	
			P-Ch	2.3	2.3	

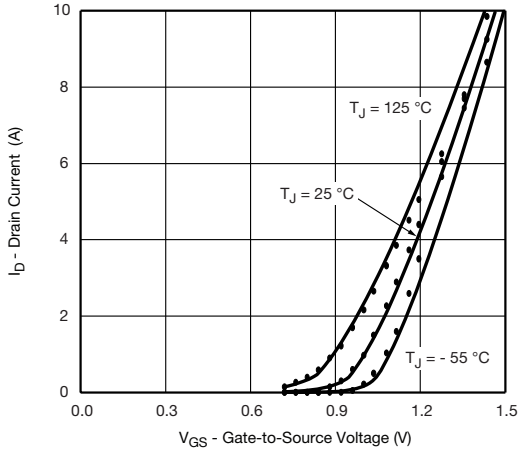
Notes

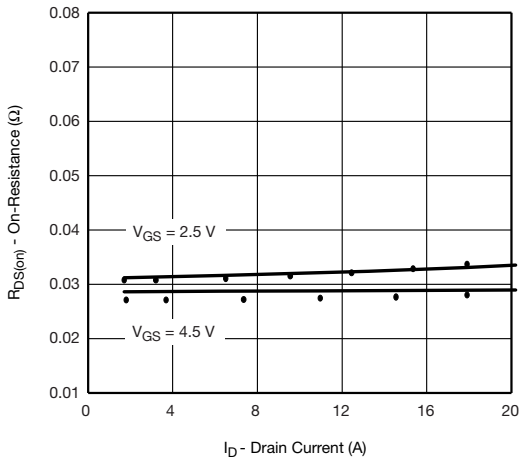
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

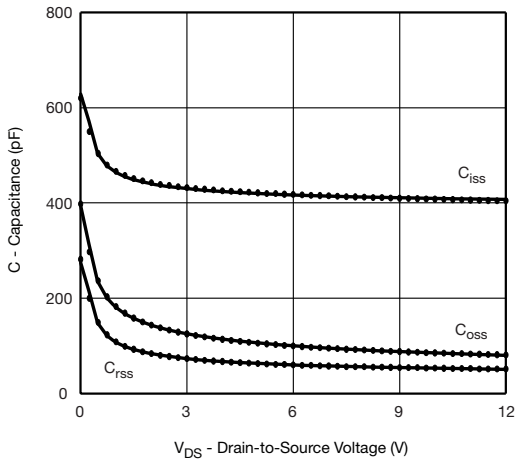
b. Guaranteed by design, not subject to production testing.

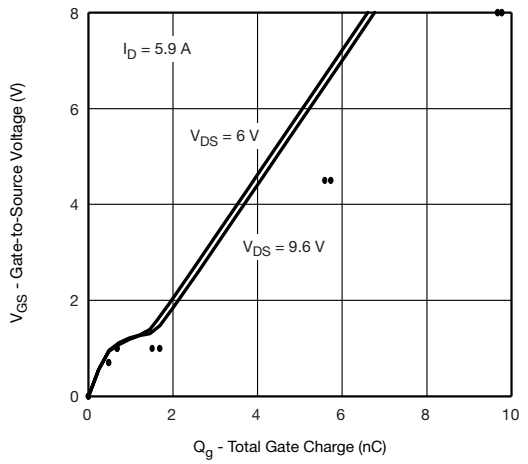
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted
N-Channel MOSFET

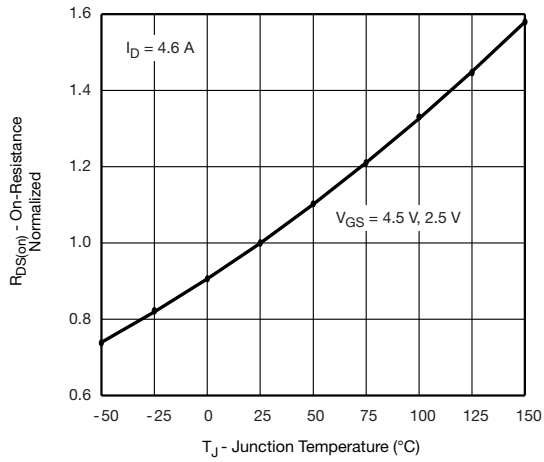








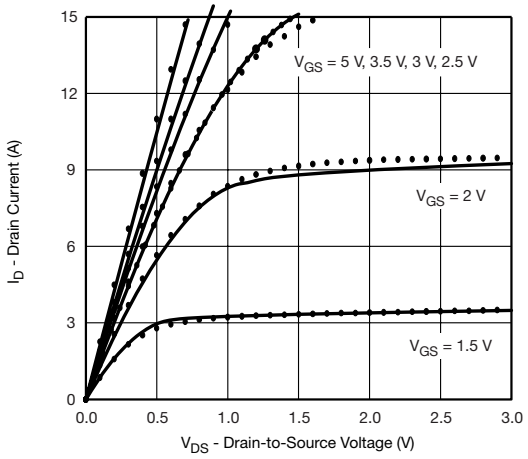


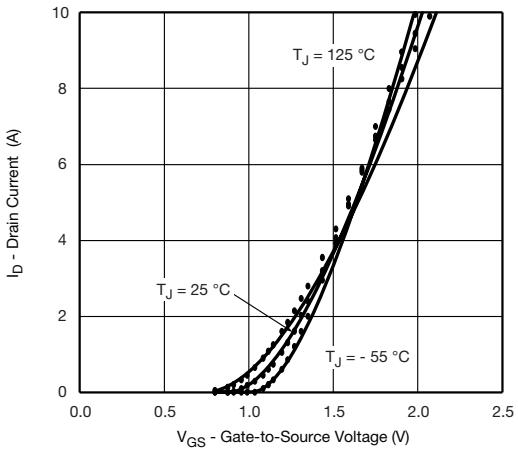


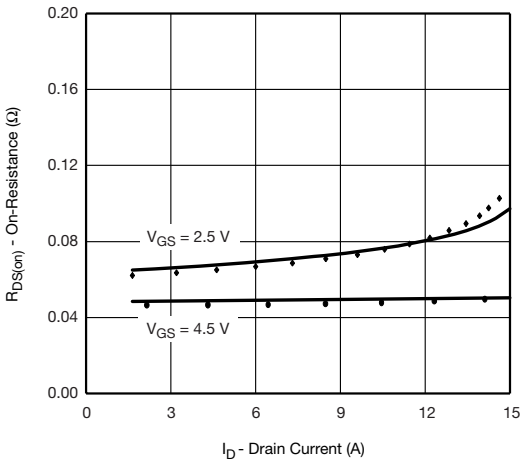
Note
Dots and squares represent measured data.

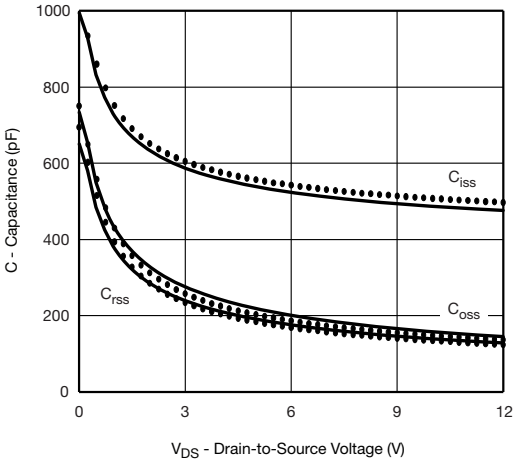
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

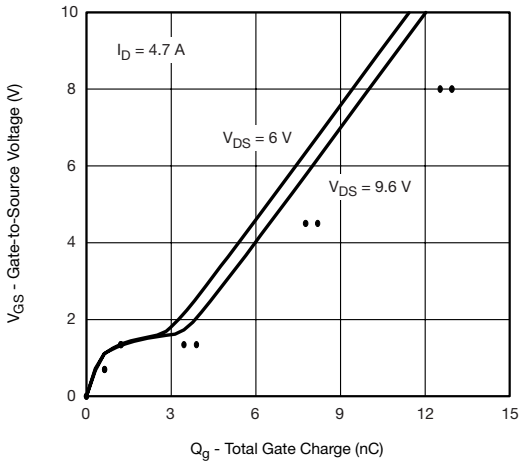
P-Channel MOSFET

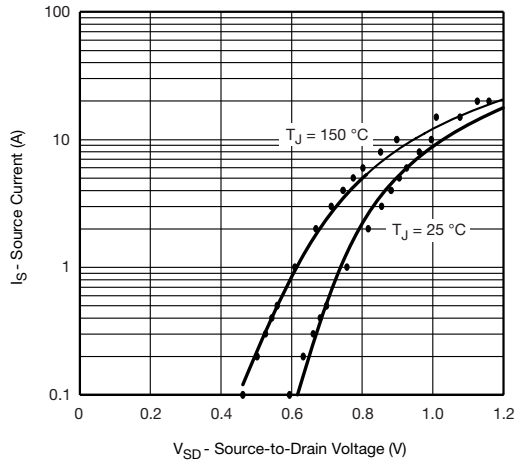












Note

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